Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	read adj delay adj adjustment	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:21
L2	0	1 and sense and delay	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:20
L3	7	self-timed adj decoder	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:29
L4	5	3 and delay	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:24
L5	1	4 and sense	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:24
L6	4	4 and read	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:24
L7	14764	6 adn dealy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:24
L8	5	4 and delay	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:28

L9	0	8 and adjust$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:25
L10	4	8 and read	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:29
L11	0	8 and read adj time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:29
L12	8	self-timed adj decod$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:29
L13	8	self-timed adj decod$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:30
L14	7806076	13 and read dj time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:30
L15	0	13 and read adj time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:30
L16	0	8 and read adj delay	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:30

L17	992	read adj delay	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:30
L18	0	17 and self-tim$3 adj decod$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:31
L19	14	17 and self-tim$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:52
L20	0	read adj margin adj adjust	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:52
L21	1	read adj margin adj adjust$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/22 14:52

US-PAT-NO: 6172530

DOCUMENT-IDENTIFIER: US 6172530 B1

TITLE: . Decoder for generating N output signals from two or more precharged input signals

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Drawing Description Text - DRTX (3):
FIG. 1 illustrates how a self-timed decoder in accordance with preferred embodiments of the present invention may be used to generate N output signals for use by domino logic in dependence on two input signals;

Drawing Description Text - DRTX (4):
FIG. 2 is a block diagram illustrating in more detail the self-timed decoder of preferred embodiments of the present invention;

Detailed Description Text - DETX (2):
FIG. 1 illustrates a self-timed decoder 10 in accordance with preferred embodiments of the present invention, which is arranged to receive as its input an encoded N bit value over path 30, and the complement of the encoded N-bit value over path 40. Based on these two input values, the decoder 10 is arranged to produce N output signals over path 50 for use as inputs to domino logic 20. Although the self-timed decoder 10 is preferably used to generate input signals for domino logic, it will be appreciated that it may used to generate signals for other circuitry, for example to generate signals used for word-line selection for a Random Access Memory (RAM). Further details of the self-timed decoder 10 in accordance with preferred embodiments will now be discussed with reference to FIG. 2.

Detailed Description Text - DETX (3):
As shown in FIG. 2, the self-timed decoder 10 includes two basic elements. The first element is a precharged NOR gate structure 100 which is arranged to receive the encoded N-bit value and its complement over paths 30 and 40, respectively, and is also arranged to receive a clock signal over path 120.

Detailed Description Text - DETX (4):
The precharged NOR gate structure 100 is arranged to generate N intermediate signals 120 dependent on the values of the encoded N-bit input value and its complement. These N intermediate signals are then output to a second element of the self-timed decoder, namely self-timed logic 110. The self-timed logic 110 is arranged to generate N output signals from the corresponding N intermediate signals received as inputs. However, in accordance with preferred embodiments, each output signal is generated from the corresponding

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Bull et al.

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(54) **DECODER FOR GENERATING N OUTPUT SIGNALS FROM TWO OR MORE PRECHARGED INPUT SIGNALS**

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(73) Assignee: **Arm Limited**, Cambridge (GB)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/335,696**

(22) Filed: **Jun. 18, 1999**

(51) Int. Cl.[7] G11C 8/00
(52) U.S. Cl. 326/105; 365/203
(58) Field of Search 365/230.06, 203; 326/106, 105

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(57) **ABSTRACT**

A decoder is provided for generating N output signals, the decoder comprising a precharged gate structure arranged to receive two or more input signals and to generate N intermediate signals. In a precharge phase, the precharged gate structure is arranged to output the N intermediate signals at a first logic value, and in an evaluate phase the precharged gate structure is arranged to maintain a first intermediate signal at the first logic value, and to cause all other intermediate signals to transition to a second logic value. Further, self-timed logic is provided for receiving the N intermediate signals, and for generating the N output signals, the self-timed logic being arranged, during the precharge phase, to generate the N output signals at the second logic value, and during the evaluate phase to cause a first output signal corresponding to the first intermediate signal to transition to the first logic value. The self-timed logic is further arranged to generate each output signal from the corresponding intermediate signal as qualified to predetermined other intermediate signal, such that the transition of the first output signal to the first logic value is delayed by a first predetermined time after the predetermined other intermediate signal has transitioned to the second logic value.

8 Claims, 4 Drawing Sheets